WHAT IS CLAIMED IS:

1. An apparatus for providing an input output from an integrated circuit, the apparatus comprising:

an upper pair of P-channel Metal Oxide Semiconductor (PMOS) devices coupled between a power supply ($V_{DDO}$) and an I/O pad;

a lower pair of N-channel MOS devices (NMOS), coupled between the I/O pad and a ground potential;

a first bias circuit providing a first bias voltage to the first upper PMOS device when the I/O pad is in an output mode and $V_{DDO}$ voltage otherwise;

a second bias circuit providing a second bias voltage to the second lower NMOS device when the I/O pad is in an output mode and a ground voltage otherwise;

a third bias circuit providing a first fixed voltage to the second upper PMOS device when $V_{PAD}$ is less than the $V_{DDO}$ voltage and a voltage equal to $V_{PAD}$ otherwise; and

a fourth bias circuit providing a second fixed voltage when $V_{PAD}$ is less than a pre-determined value and a voltage higher than the second fixed voltage otherwise.

2. The apparatus of claim 1 further comprising a well biasing circuit which provides a well bias to the upper pair of PMOS devices.

3. The apparatus of claim 2 wherein the well biasing circuit provides a bias voltage of $V_{DDO}$ if a voltage on the I/O pad is less than $V_{DDO}$ and provides the voltage on the I/O pad as the bias voltage otherwise.

4. The apparatus of claim 1 further comprising:

a NMOS device having a drain coupled to $V_{PAD}$;

the NMOS device having a source coupled to core circuitry; and

having the gate coupled to the fourth bias voltage.